REMARKS

In section 2 of the Office Action, the Examiner rejected claims 1, 2, 5, 8, and 20-31 under 35 U.S.C. §103(a) as being unpatentable over "admitted prior art" in view of Purho.

However, even if "admitted prior art" and Purho could be combined, the combination would not meet the limitations of independent claim 1 because neither "admitted prior art" nor Purho discloses or suggests to one of ordinary skill in the art the recitations of enabling only the navigation computer to be clocked by the clock of the navigation computer at times, and of enabling both the navigation computer and the inertial measurement unit to be clocked by the clock of the navigation computer at other times.

Purho discloses a synchronization system that has a first element A with a first clock, a second element B with a second clock, and a third element C with a third clock. The second element B is located between the first and the second elements A and C and interconnects the first and the second elements A and C.

The clock of the first element A is used as a reference clock in the system. The second element B is a general-purpose processor, such as a PC. The clock of

the third element C regularly sends clock pulses cclk to the second element B.

The clock in the third element C is synchronized to the clock in the first element A and not to the clock in the second element B.

In performing this synchronization, offsets between the clock in the third element C and the clock in the first element A are periodically determined by the second element B. In order to calculate these offsets, the second element B sends a synchronization packet spkt to the first element A upon receiving a clock pulse cclk from the third element C, and the first element A responds by sending a response packet rpkt to the second element B. The synchronization packet spkt and the response packet rpkt contain various timestamps.

These timestamps indicate the time at which the synchronization packet spkt is transmitted by the second element B, the time at which the first element A receives the synchronization packet spkt, the time at which the first element A sends the response packet rpkt to the second element B. Also, the second element determines the time at which the response packet rpkt is received by the second element B. In order to generate a timestamp indicating the time at which the response packet rpkt is

received at the second element B, the second element B counts the number of clock pulses cclk received from the third element C beginning at the point when the synchronization packet spkt is transmitted by the second element B to the first element A. Any fractional time is determined according to the internal clock of the second element B.

The offsets are determined from these timestamps. The offsets are used by the second element B to cause adjustments of the clock in the third element C by way of a correction message cmsg. The correction message cmsg indicates how much the clock of the third element C must be advanced or retarded in order to maintain a clock pulse cclk rate synchronous to the clock pulse rate of the clock in the first element A.

If applicants understand the Examiner's argument correctly, the Examiner argues that the second element B of Purho enables only the first element A to be clocked at times by the clock of the first element A (this clock is described in Purho as the reference clock), and that the second element B enables both the first element A and the third element C to be clocked at other times by the clock of the first element A.

However, Purho discloses no such thing.

Instead, Purho discloses that each element A, B, and C is clocked by its own clock. The second element B merely synchronizes the clocks of the elements A and C to one another. The second element B does not enable the clock of one element to clock another element. That is, the clock of the first element A is not used to clock the third element C, and the clock of the third element C is not used to clock the first element A.

Accordingly, because neither "admitted prior art" nor Purho discloses or suggests enabling only a first device to be clocked by the clock of the first device at times, and enabling both the first device and a second device to be clocked by the clock of the first device at other times, "admitted prior art" and Purho taken together would not suggest the invention of independent claim 1 to one of ordinary skill in the art.

For this reason, independent claim 1 is not unpatentable over "admitted prior art" in view of Purho.

For similar reasons, neither "admitted prior art" nor Purho discloses or suggests supplying a first clock signal from a clock of a first device only to the first device in response to a first condition, supplying the first clock signal from the clock of the first device to the first device and to a second device in response to

a second condition, and supplying a clock signal from a third device to the first, second, and third devices in response to a third condition, all as required by independent claim 20.

Thus, "admitted prior art" and Purho taken together would not suggest the invention of independent claim 20 to one of ordinary skill in the art.

For this reason, independent claim 20 is not unpatentable over "admitted prior art" in view of Purho.

Because independent claims 1 and 20 are not unpatentable over "admitted prior art" in view of Purho, dependent claims 2, 5, 8, and 21-31 are likewise not unpatentable over "admitted prior art" in view of Purho.

In section 3 of the Office Action, the Examiner rejected claims 3, 4, and 12-14 under 35 U.S.C. §103(a) as being unpatentable over "admitted prior art" in view of Purho and further in view of Akopian.

Akopian likewise fails to disclose or suggest enabling only a first device to be clocked by the clock of the first device at times, and enabling both the first device and a second device to be clocked by the clock of the first device at other times.

Accordingly, "admitted prior art" and Purho and Akopian taken together would not suggest the invention of

independent claim 1 to one of ordinary skill in the art. For this reason, independent claim 1 is not unpatentable over "admitted prior art" in view of Purho and further in view of Akopian.

Because independent claim 1 is not unpatentable over "admitted prior art" in view of Purho and further in view of Akopian, dependent claims 3 and 4 are likewise not unpatentable over "admitted prior art" in view of Purho and further in view of Akopian.

Independent claim 12 requires the selective supply of a clock signal to only a first device and to both the first device and a second device.

As indicated above, "admitted prior art" and Purho and Akopian taken together do not disclose or suggest selectively supplying a clock signal to only a first device and to both the first device and a second device.

Accordingly, "admitted prior art" and Purho and Akopian taken together would not suggest the invention of independent claim 12 to one of ordinary skill in the art. For this reason, independent claim 12 is not unpatentable over "admitted prior art" in view of Purho and further in view of Akopian.

Because independent claim 12 is not unpatentable over "admitted prior art" in view of Purho and further in view of Akopian, dependent claims 13 and 14 are likewise not unpatentable over "admitted prior art" in view of Purho and further in view of Akopian.

CONCLUSION

In view of the above, it is clear that the claims of the present application are patentable over the references applied by the Examiner. Accordingly, allowance of these claims and issuance of the above captioned patent application are respectfully requested.

Respectfully submitted,

Schiff Hardin LLP
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
(312) 258-5500
Customer No. 000128

By: _____
Trevor B. Joike
Reg. No: 25,542

March 7, 2006